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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,688	11/18/2003	Peter A. Sandon	END920030075US1	4804

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ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,688	SANDON ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-30 have been examined.

Acknowledgment of papers filed: oath, specification, drawings, and IDS, on November 18th, 2003. The papers filed have been placed on record.

Specification

2. The title is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. Claims 9-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 9-17 are method claims, but contain no essential steps for accomplishing a method. For the purpose of art rejections under 35 USC 102 in this office action, claims 9-17 will be treated as apparatus claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-20, 23,27 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Access and Alignment of Data in an Array Processor (herein Lawrie).

6. Regarding claims 1 and 9, Lawrie discloses a processor, comprising M independent vector register files (page 99 introduction paragraph 1), said M vector register files adapted to collectively store a matrix of L data elements (page 99 section II second paragraph),

Note that registers in a particular column are considered to be a register file.

Each data element having B binary bits, said matrix having N rows and M columns, said L=N*M (page 99 section II second paragraph line 3), each column having K subcolumns (page 108 lines 11-14),

Note that the partitians mentioned are considered to be subcolumns. Another possible interpretation would allow the column itself to be a subcolumn. See below.

Said N.gtoreq.2, said M.gtoreq.2 (page 99 section II second paragraph line 3), said K.gtoreq.1,

Note that, as indicated by this claim, since K = 1 in some instances, it is reasonable to view a subcolumn as an entire column.

Said B.gtoreq.1, each row of said N rows being addressable (page 99 section II second paragraph lines 4-6), each subcolumn of said K subcolumns being addressable (page 108 lines 11-14), said processor not adapted to duplicatively store said L data elements (page 100 fig 2).

Note that, after viewing Applicant's specification, it appears that this claim is referring to paragraph 63 of Applicant's detailed description. Paragraph 63 discloses that the matrix information is not required to be duplicated for functional addressability. Consequently, the term "processor not adapted to duplicatively store said L data elements" will be interpreted in that way. Figure 2 of the reference shows a 2X2 matrix which, as shown in 1-skew storage, does not require duplicated information.

7. Regarding claims 2 and 10, Lawrie discloses the processor of claims 1 and 9, wherein the processor further comprises M address registers (page 99 section II second paragraph), wherein each address register of the M address registers is associated with a corresponding one of the M vector register files (page 99 section II second paragraph lines 4-6),

Note that, as indicated by the citation, each column is addressable, giving the address register a correspondance to each of the M vector register files.

Wherein each of the M vector register files includes an array of N registers (page 99 section II second paragraph line 3), wherein each of the N*M registers of the M vector register files are adapted to store a data element of the L data elements (page 100 fig 2), and wherein each vector register file is independently addressable through its associated address register being adapted to point to one of the N registers of said vector register file (page 99 section II second paragraph lines 4-6).

8. Regarding claims 3 and 11, Lawrie discloses the processor of claims 2 and 10, wherein the data elements of each subcolumn are adapted to be stored in different vector register files, and wherein the data elements of each row are adapted to be stored in different vector register files (page 100 col 1 second paragraph).

Note that, as with most any register file, there is no limitations to rearranging the information stored in memory. Using storing and load instructions, any set of information can be stored in a plurality of different configurations within the register file.

9. Regarding claims 4 and 12, Lawrie discloses the processor of claims 3 and 11, wherein the data elements of each subcolumn are adapted to be stored in different relative register locations of the different vector register files, and wherein the data elements of each row are adapted to be stored in a same relative register location of the different vector register files (page 100 col 1 second paragraph).

See claim 3.

10. Regarding claims 5 and 13, Lawrie discloses the processor of claims 3 and 11, wherein the processor further comprises M multiplexors respectively coupled to the M vector register files (page 100 col 1 second paragraph and page 103 figure 7),

Note that, according to Wordnet ® 2.0 © 2003 Princeton University, a multiplexor is "a device that can interleave two or more activities"; therefore, the mechanism used to choose what values are put into the register file, a mechanism that must exist in this invention, is considered to include a multiplexor for each element.

And wherein if the matrix is stored in the M vector register files then: the M multiplexors are adapted to respond to a command to read a row of the matrix by mapping the data elements of the row from the M vector register files to the row of the matrix in accordance with a read-row mapping algorithm (page 108 lines 11-14); and the M multiplexors are adapted to respond to a command to read a subcolumn of the matrix by reading the data elements of the subcolumn from the M vector register files to the subcolumn of the matrix in accordance with a read-subcolumn mapping algorithm (page 108 lines 11-14).

Note that, with little clarification in Applicant's specification, the "write subcolumn mapping algorithm" and "write-row mapping algorithm" are considered to be no more than the logic necessary to allow the subcolumn and rows, respectively, to be adequately accessed.

11. Regarding claims 6 and 14, Lawrie discloses the processor of claims 3 and 11, wherein the processor further comprises M multiplexors respectively coupled to the M vector register files (page 100 col 1 second paragraph);

Note that, according to Wordnet ® 2.0 © 2003 Princeton University, a multiplexor is "a device that can interleave two or more activities"; therefore, the mechanism used to choose what values are put into the register file, a mechanism that must exist in this invention, is considered to include a multiplexor for each element.

Wherein the M multiplexors are adapted to respond to a command to write a row of the matrix by mapping the data elements of the row to the M vector register files in

accordance with a write-row mapping algorithm (page 108 lines 11-14); and wherein the M multiplexors are adapted to respond to a command to write a subcolumn of the matrix by mapping the data elements of the subcolumn to the M vector register files in accordance with a write-subcolumn mapping algorithm (page 108 lines 11-14).

Note that, with little clarification in Applicant's specification, the "write subcolumn mapping algorithm" and "write-row mapping algorithm" are considered to be no more than the logic necessary to allow the subcolumn and rows, respectively, to be adequately accessed.

12. Regarding claims 7 and 15, Lawrie discloses the processor of claims 2 and 10, wherein the processor further comprises M multiplexors respectively coupled to the M vector register files such that each of the M multiplexors has a different value (page 100 col 1 second paragraph).

Note that, according to Wordnet ® 2.0 © 2003 Princeton University, a multiplexor is "a device that can interleave two or more activities"; therefore, the mechanism used to choose what values are put into the register file, a mechanism that must exist in this invention, is considered to include a multiplexor for each element.

13. Regarding claim 8, Lawrie discloses the processor of claim 1, wherein the matrix of L data elements are stored in the M vector register files (page 99 second II paragraph 2, lines 2-6 and fig 2).

14. Regarding claim 16, Lawrie discloses the method of claim 9, further comprising addressing a row of the N rows.

15. Regarding claim 17, Lawrie discloses the method of claim 9, further comprising addressing a subcolumn of the K*M subcolumns (page 108 lines 11-14).

16. Regarding claims 18 and 25, Lawrie discloses a processor, comprising M independent vector register files (page 99 introduction paragraph 1), said M vector register files adapted to collectively store a matrix of L data elements (page 99 section II second paragraph), each data element having B binary bits, said matrix having N rows and M columns, said L=N*M (page 99 section II second paragraph line 3), each column having K subcolumns (page 108 lines 11-14), said N.gtoreq.2, said M.gtoreq.2 (page 99 section II second paragraph line 3), said K.gtoreq.1, said B.gtoreq.1, each row of said N rows being addressable (page 99 section II second paragraph lines 4-6), each subcolumn of said K subcolumns being addressable (page 108 lines 11-14),

See claim 1.

Said matrix including a set of arrays such that each array is a row or subcolumn of the matrix (fig 2), said processor adapted to execute an instruction that performs an operation on a first array of the set of arrays, said operation being performed with selectivity with respect to the data elements of the first array (page 99 introduction paragraph 1).

17. Regarding claims 19 and 26, Lawrie discloses the processor of claims 18 and 25, wherein the processor further comprises M multiplexors respectively coupled to the M vector register files, and wherein the values associated with the M multiplexors control said selectivity (page 100 col 1 second paragraph).

Note that, according to Wordnet ® 2.0 © 2003 Princeton University, a multiplexor is "a device that can interleave two or more activities"; therefore, the mechanism used to choose what values are put into the register file, a mechanism that must exist in this invention, is considered to include a multiplexor for each element.

18. Regarding claims 20 and 27, Lawrie discloses the processor of claims 18 and 25, wherein the processor further comprises M address registers (page 99 and 100 section II), wherein each address register of the M address registers is associated with a corresponding one of the M vector register files (page 108 lines 11-14),

Note that the rows are accessable, suggesting they are addressable, further suggesting that there is an "address register" for each register file (or row).

Wherein each of the M vector register files includes an array of N registers (page 99 and 100 section II), wherein each of the N*M registers of the M vector register files are adapted to store a data element of the L data elements (page 99 and 100 section II), and wherein each vector register file is independently addressable through its associated address register being adapted to point to one of the N registers of said vector register file (page 108 lines 11-14).

19. Regarding claims 23 and 30, Lawrie discloses the processor of claims 18 and 25, wherein the processor is not adapted to duplicatively store the L data elements (page 100 fig 2).

See claim 2.

20. Regarding claim 24, Lawrie discloses the processor of claim 18, wherein the matrix of L data elements are stored in the M vector register files (page 100 col 1 second paragraph).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 21-22 and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawrie in view of AMD 64-bit Technology (herein AMD).

Regarding claims 21 and 28, Lawrie discloses the processor of claim 18 and the use of instructions utilizing the memory matrix (page 99 introduction).

Lawrie fails to disclose enough detail about the types of instructions used.

AMD discloses a vector-shift instruction being supported (page 135 last paragraph, second to last line) and a vector move instruction (page 137 section 4.2.5 first paragraph).

It is expected that one of ordinary skill in the art would have realized the advantages of utilizing a shift and move instruction. Both of these instructions are fairly standard in most instruction sets because they give the programmer the ability to rearrange and interchange vector registers in a single instruction, steps that are often times essential while programming software to be utilized on a processor. AMD even discloses that "Move instructions...are among the most frequently used instructions in 128-bit media procedures" (page 137 section 4.2.5 first three lines). Examiner asserts that shift instructions are also commonly utilized by programmers. For these reasons, Lawrie would be motivated to include these instructions in the instruction set of the referenced invention.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the processing system of Lawrie to include vector-move and vector-shift instructions in order to have instructions that "insert an exact copy of the first array into the second array" and "rearrange the data elements of the first array within the first array", respectively.

Conclusion

23. The following is text cited from 37 CFR 1.11(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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